SELECTABLE SINGLE MODE OR DIFFERENTIAL MODE OPERATION IN A SINGLE AMPLIFIER

FIELD OF THE INVENTION

The present invention relates to an amplifier using common output terminals for dual modes of operation.

BACKGROUND OF THE INVENTION

Certain integrated circuit (IC) chips have the ability to internally generate differential signals that are driven off chip. These differential signals take the form of the original differential signal or can be converted to a single ended signal. In order to provide the capability of either output, the IC chips use parallel output paths. One path drives the signal through a differential amplifier, maintaining the original form of the signal. The other path is used to transmit the differential pair to be driven off chip to an amplifier that converts it to a single ended signal. For configurations consisting of two differential signals, four pads on the IC chip are required, one pair of pads for the differential signal mode (both differential signals are identical) and two pads for the signals in the single ended mode. If the IC is required to function only in one mode at any given time, use of four pads can increase the complexity of the IC chip by consuming additional space for redundant pads that could otherwise be used for pads providing other output signals.

Accordingly, a need exists for a dual mode amplifier having a simplified output configuration.

SUMMARY OF THE INVENTION

A first amplifier having dual modes of operation includes two differential amplifiers each receiving a pair of differential input signals and having an output terminal. Circuitry couples the differential amplifiers together and is controlled by a control signal. A first value of the control signal activates the circuitry so that the differential amplifiers can provide a differential signal at the output terminals in response to the differential input signals. A second value of the control signal deactivates the circuitry so that the differential amplifiers can operate independently to provide a pair of single ended signals at the output terminals in response to two differential input signals.

A second amplifier having dual modes of operation also includes two differential amplifiers each receiving a pair of differential input signals and having an output terminal. The second amplifier includes coupling circuits, controlled by a control signal, for coupling together corresponding differential input signals. A first value of the control

signal activates the coupling circuits so that the differential amplifiers provide a differential signal at the output terminals in response to the differential input signals. A second value of the control signal deactivates the coupling circuits so that the differential amplifiers operate independently to provide a pair of single ended signals at the output terminals in response to two differential input signals.

These exemplary first and second amplifiers can also be used to implement a method for providing dual modes of operation in an amplifier using only one set of output terminals.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings are incorporated in and constitute a part of this specification and, together with the description, explain the advantages and principles of the invention.

FIG. 1 is a diagram illustrating an integrated circuit chip containing a dual mode amplifier.

FIG. 2 is a circuit diagram of a dual mode amplifier.

FIG. 3 is a circuit diagram of an alternate embodiment of a dual mode amplifier.

FIG. 4 is a diagram of an exemplary input signal to a dual mode amplifier.

FIG. 5 is a diagram of an exemplary output signal to a dual mode amplifier with synchronization.

FIG. 6 is a diagram of an exemplary output signal to a dual mode amplifier without synchronization.

DETAILED DESCRIPTION

FIG. 1 is a diagram illustrating an IC chip 10 containing a dual mode amplifier 12. IC chip 10 includes circuitry 14 that uses dual mode amplifier 12 to drive signals off chip via pads 16 and 18. Many IC chips use dual mode amplifiers and, therefore, an implementation of circuitry 14 will depend upon the type of IC chip in which it is contained. The configuration of dual mode amplifier 12, as explained below, requires only two pads 16 and 18 for providing the output signals in both modes, obviating the need for different pads for each mode. The term pad includes any type of terminal or connection for providing a signal off chip.

Dual mode amplifier 12 operates in two modes. In a first mode, it provides two single ended signals at pads 16 and 18 operating independently of one another. In a second mode, it provides differential output signals at pads 16 and 18. Thus, the first mode is referred to as a singled ended mode, and the second mode is referred to as a

differential mode. The terms singled ended mode and differential mode are used only as labels, and the same or equivalent modes can be referred to by other terminology.

FIG. 2 is a circuit diagram of one embodiment of dual mode amplifier 12. Amplifier 12 includes two differential amplifiers 20 and 22. Amplifier 20 includes transistors 26 and 34 connected in series, transistors 28 and 36 connected in series, and the series pairs connected in parallel. Amplifier 22 includes transistors 54 and 60 connected in series, transistors 52 and 64 connected in series, and the series pairs connected in parallel. In differential amplifier 20, transistors 26 and 34 drive an output signal (OUTPUTn) on line 30, and in differential amplifier 22, transistors 54 and 60 drive an output signal (OUTPUTp) on line 58. Lines 30 and 58 are connected to pads 16 and 18, providing terminals or connections for driving signals off chip.

The gate terminals of the sink transistors 28 and 64 are connected via a line 66. A coupling transistor 46 connects differential amplifiers 20 and 22. Transistors 40 and 44, the gates of which are connected via line 42, provide for current source biasing for differential amplifiers 20 and 22, respectively.

Amplifier 12 may optionally include coupling transistors to reduce distortion in the output signals. These include transistors 70 and 72 connected in parallel and coupling the gate terminals of transistors 34 and 52, and transistors 78 and 80 connected in parallel and coupling the gate terminals of transistors 36 and 54. In the embodiment shown in FIG. 2, coupling transistors 70, 72, 78, and 80 are not absolutely necessary. However, they can reduce distortion in the output signals of amplifier 12, as explained below, and thus enhance its performance.

The inputs to amplifier 12 include two sets or pairs of differential signals, one pair includes signals A0p and A0n, and the other pair includes signals A1p and A1n. As shown, those inputs are provided at the gate terminals of transistors 34, 36, 52, and 54, respectively. The dual modes of operation are controlled by a control signal, in this example the select signal (SEL). The particular mode of operation, single ended or differential ended, is controlled by first and second values of the select signal SEL, in this example a first value equal to ground (GND) and a second value equal to the power supply value (VDD). Alternatively, other values may be used, and the value for the power supply VDD may depend upon a particular implementation.

In the single ended mode of operation, the select signal SEL is set to ground, and the nSEL signal is set to the power supply value VDD. In this single ended mode, each differential amplifier 20 and 22 operates independently, converting the two differential

pair input signals into two singled ended output signals. In particular, differential amplifier 20 converts differential pair input signals A0p and A0n to a single ended output signal (OUTPUTn) on line 30, and differential amplifier 22 converts differential pair input signals A1p and A1n to a single ended output signal (OUTPUTp) on line 58. In this mode, signals OUTPUTn and OUTPUTp operate independently of one another.

In the single ended mode, the sink transistors 28 and 64 are active due to the inverted ground signal (inverted SEL = GND) input to their gate terminals. The coupling transistor 46 is deactivated in the singled ended mode, due to the ground signal (SEL = GND) at its gate terminal, de-coupling differential amplifiers 20 and 22. The optional coupling transistors 70, 72, 78, and 80 are also deactivated due to the ground signals (SEL = GND and inverted nSEL = VDD) input to their gate terminals, deactivating the bias distortion circuitry, when used, for the singled ended mode so that each differential amplifier 20 and 22 can operate independently.

The term activate or active means that the corresponding transistor or other circuit element is on and capable of transmitting current. The term deactivate or deactive means that the corresponding transistor or other circuit element is off and not capable of transmitting current, aside from any negligible current due to leakage or other factors.

In the differential mode of operation, the two pairs of differential input signals, first pair A0p and A0n, and second pair A1p and A1n, are identical from their sources. In this differential mode, the select signal SEL is set to the power supply value VDD, and the nSEL signal is set to ground. The sink transistors 28 and 64 are deactivated due to the ground signal (inverted SEL = VDD) input to their gate terminals. The coupling transistor 46 is active in the differential mode due to the power supply signal (SEL = VDD) input to its gate terminal. With coupling transistor 46 being active, differential amplifiers 20 and 22 operate together (not independently) in order to provide a differential signal at lines 30 and 58 as signals OUTPUTn and OUTPUTp in response to the differential input signals.

Optional coupling circuits can help reduce distortion in the output signals for the differential mode of operation. In particular, the coupling circuits can include, for example, the optional coupling transistors 70, 72, 78, and 80, which are active in the differential mode due to the power supply signal (SEL = VDD and inverted nSEL = GND) input to their gate terminals. Being active, transistors 70 and 72 effectively provide a short between the gate terminals of transistors 34 and 52, eliminating or at least substantially reducing timing differences in the input signals A0p and A1p resulting from

distortion or other factors. Likewise, transistors 78 and 80, being active, effectively provide a short between the gate terminals of transistors 36 and 54, eliminating or at least substantially reducing timing differences in the input signals A0n and A1n resulting from distortion or other factors. Therefore, these optional coupling transistors 70, 72, 78, and 80, when used, can reduce distortion in the differential mode by coupling and hence time synchronizing corresponding differential input signals.

FIG. 3 is a circuit diagram of an alternate embodiment of dual mode amplifier 12. The embodiment in FIG. 3 includes two differential amplifiers 90 and 92, similar to differential amplifiers 20 and 22, except that they do not include sink transistors 28 and 64, and also are not linked by coupling transistor 46. Also, the embodiment in FIG. 3 requires the coupling transistors 70, 72, 78, and 80, or equivalent circuitry.

In the alternate embodiment, transistors 40 and 44, having their gate terminals connected via line 42, provide current source biasing for differential amplifiers 90 and 92. As in the other embodiment, transistors 26 and 34 drive an output signal (OUTPUTn) on line 30 in differential amplifier 90, and transistors 54 and 60 drive an output signal (OUTPUTp) on line 58 in differential amplifier 92. The inputs to amplifier 12 in the alternate embodiment include the two sets of differential signals, first pair A0p and A0n, and second pair A1p and A1n; those inputs are provided at the gate terminals of transistors 34, 36, 52, and 54, respectively.

In the single ended mode of operation in the alternate embodiment, the select signal SEL is set to ground, and the nSEL signal is set to the power supply value VDD. As in the other embodiment, in this single ended mode, each differential amplifier 90 and 92 operates independently, converting the two differential pair input signals into two singled ended output signals. In particular, differential amplifier 90 converts differential pair input signals A0p and A0n to a single ended output signal (OUTPUTn) on line 30, and differential amplifier 92 converts differential pair input signals A1p and A1n to a single ended output signal (OUTPUTp) on line 58. In this mode, signals OUTPUTn and OUTPUTp operate independently of one another. Also, the coupling circuits, implemented with coupling transistors 70, 72, 78, and 80 in this example, are deactivated in this mode due to the ground signal (SEL = GND and inverted nSEL = VDD) input to their gate terminals, decoupling differential amplifiers 90 and 92 so they can operate independently in the single ended mode.

In the differential mode of operation in the alternate embodiment, the two pairs of differential input signals, first pair A0p and A0n, and second pair A1p and A1n, are

identical from their sources. In this differential mode, the select signal SEL is set to the power supply value VDD, and the nSEL signal is set to ground. The coupling circuits, implemented with coupling transistors 70, 72, 78, and 80 in this example, are active in the differential mode due to the power supply signal (SEL = VDD and inverted nSEL = GND) input to their gate terminals. Being active, transistors 70 and 72 effectively provide a short between the gate terminals of transistors 34 and 52, eliminating or at least substantially reducing timing differences in the input signals A0p and A1p. Likewise, transistors 78 and 80 effectively provide a short between the gate terminals of transistors 36 and 54, eliminating or at least substantially reducing timing differences in the input signals A1p and A1n. Therefore, these coupling transistors 70, 72, 78, and 80, in the alternate embodiment, couple each pair of differential input signals to provide differential output signals at lines 30 and 58 as signals OUTPUTn and OUTPUTp.

In both embodiments shown in FIGS. 2 and 3, a power control signal (PCNTRL) input to the gate terminals of transistors 26 and 60 is used to toggle off and on a load PFET (26 and 66) or other circuit element, typically on when amplifier 12 is in a voltage mode and off when amplifier 12 is in a current mode. In the voltage mode, the differential amplifiers 20 and 22 (or 90 and 92) provide single or differential ended voltages at lines 30 and 58 for the output signals. In the voltage mode, the differential amplifiers 20 and 22 (or 90 and 92) provide single or differential ended currents at lines 30 and 58 for the output signals.

Although amplifier 12 in both embodiments is shown as implemented using field effect transistors (FETs), it can alternatively be implemented with other types of transistors or circuit elements providing the same or equivalent functions.

In addition, the embodiments shown in FIGS. 2 and 3, or equivalent embodiments, can be used to implement a method for providing dual modes of operation in an amplifier using only one set of output terminals. The method can include the steps of, for example, receiving first and second pairs of differential input signals, the first pair A0p and A0n, and the second pair A1p and A1n, and using a control signal to provide the dual modes of operation. In particular, the using step can include, for example, providing, based upon a first value of the control signal SEL, a differential signal at first and second output terminals at lines 30 and 58 in response to the first and second pair of differential input signals, and providing, based upon a second value of the control signal SEL, single ended signals at the first and second output terminals at lines 30 and 58 in response to the first and second pair of differential input signals, respectively.

FIG. 4 is a diagram of an exemplary input signal 94 to dual mode amplifier 12. FIG. 5 is a diagram of an exemplary output signal 95, based upon input signal 94, of dual mode amplifier 12 with synchronization using coupling transistors 70, 72, 78, and 80 in the embodiment of FIG. 2. With the coupling transistors used to reduce distortion, the differential signals cross at a point 96 at approximately 50% of the difference in amplitude (93) between the signals. For example, with a 400 milliVolt (mV) amplitude difference (93), the cross-over point 96 will be at approximately 200 mV between the signals.

FIG. 6 is a diagram of an exemplary output signal 97 to dual mode amplifier 12 without synchronization, meaning without using coupling transistors 70, 72, 78, and 80 in the embodiment of FIG. 2. Without the synchronization provided by these coupling transistors, the differential signals may cross over at a point (98) substantially not equal to approximately 50% of the difference in amplitude between the signals and at variable points away from the 50% value. This variable cross-over point may result from, for example, noise within the circuit. Therefore, although the coupling transistors are not necessary, they can provide for reduced noise and more consistent differential output signals by time synchronizing the input signals.

The time between pulses, pulse width 99, can vary based upon a particular implementation and requirements for the output signals. For example, a high performance output may have a pulse width of 625 picoseconds (ps) ±8 ps, while a low performance output may have a pulse width of 800 ps ±20 ps. A low performance output may be used with, for example, a memory IC chip, and a high performance output may be use with, for example, an application specific integrated circuit. These exemplary pulse widths, heights, and applications are provided for illustrative purposes only; dual mode amplifier 12 can provide outputs having any particular pulse widths and heights, used for any application.

While the present invention has been described in connection with an exemplary embodiment, it will be understood that many modifications will be readily apparent to those skilled in the art, and this application is intended to cover any adaptations or variations thereof. For example, various types of circuit components and configurations may be used without departing from the scope of the invention. This invention should be limited only by the claims and equivalents thereof.